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MITSUBISHI DENKI K.K.

Translation of the Office Action

Re: Request for substantive examination effectively filed on **July 25, 2001 (date of payment)**

The examination of the above-identified patent application has led to the results as elucidated below.

For a response, a term of **4 months** has been set, starting from the date of service.

Two separate copies must be submitted of any documents enclosed to the response statement (e.g. patent claims, specification, parts of the specification, drawings). Only one copy is required of the response statement itself.

If the patent claims, the specification or the drawings are modified in the course of the proceedings, the applicants are - if the modifications are not suggested by the German Patent and Trademark Office - requested to indicate in detail the passage(s) of the original documents disclosing the inventive features described in such new documents.

In this office action, the following references are cited for the first time (the consecutive numbering of which will be maintained throughout the further proceedings):

1) DE 693 28 084 T2
2) WO 98/37656 A2
3) US 6,100,733 A
4) DE 691 13 836 T2
5) EP 0 704 975 A1
6) US 5,796,673 A

I

Reference 1) (cf. especially Fig. 1 and the relating parts of the description) discloses a delay locked loop (32, 36, 40, 44 50, 56 and 58) comprising:

* a delay circuit (40, 44 and 50) delaying a first clock (exit of 42) to output a second clock (exit of 50);
* a detector (56, 58) detecting a phase difference between said first and second clocks; and

* a gray code counter (36) responsive to an output of said detector (56, 58) for generating a signal (38) adjusting an amount of delay of said delay circuit (page 7, lines 7 to 12).

Hence, the device of claim 1 with all its features is already known from reference 1). Therefore, claim 1 is not allowable due to lack of novelty.

II

Reference 2) (cf. especially Fig. 3 and the relating parts of the description) discloses a semiconductor device (page 1, indication of DRAMs) comprising a DLL (delay locked loop) (Figure 3) which - according to independent claim 4 - includes an input buffer (202), a delay circuit (210), a detector (220) and a counter (240). Reference 2) does not explicitly indicate which type of counter is supposed to be used. However, it belongs to the scope of expert skill to use, if necessary, a gray code counter. Moreover, this is obvious to the person skilled in the art because he knows corresponding control circuit using a gray code counter (cf. e.g. in reference 1)).

Therefore, independent claim 4 is not allowable due to lack of an inventive step.

Reference 3) (cf. especially Fig. 2 and the relating parts of the description) discloses a semiconductor device (colum 1, lines 25 et seq., indication of DDR SDRAMs) comprising a DLL (Fig. 2) which - according to independent claim 11 - includes a first input buffer and a second input buffer (column 1, lines 63 to 67) for generating first and second internal clock signals (CLK1, CLK2), a first delay circuit and a second delay circuit (4, 5) for generating third and fourth internal clock signals

(CLK1', CLK2'), and a phase detector (2). Reference 3) does not explicitly indicate how the phase error signal of the phase detector is converted into a signal controlling the delay circuits. However, also to this respect, it belongs to the scope of expert skill to use, if necessary, a gray code counter. Moreover, this is obvious to the person skilled in the art because he knows corresponding control circuit using a gray code counter (cf. e.g. in reference 1)).

Therefore, independent claim 11 is not allowable either due to lack of an inventive step.

The method steps indicated in independent claim 14 are merely a indication of use of the device features indicated in claim 1. Therefore, independent claim 14 is not allowable either due to lack of novelty.

III

The conversion of a gray code into a binary code according to claims 2, 5 and 15 is known to the person skilled in the art from reference 4) (Fig. 1).

The use of a fine delay element and of a coarse delay element according to claims 3 and 6 is known to the person skilled in the art from reference 5) (Fig. 3).

The features of claims 7 to 10, 12, 13, 16 and 17 concerning the data input, the temporary storage and the data output in an SDRAM are generally familiar to the person skilled in the art (cf. e.g. in reference 6): Fig. 1, 3 and 5).

Those features of the subclaims which are not indicated by prior art publications are merely simple developments lacking any inventive merit of their own.

IV

Therefore, the prospect of granting a patent cannot be held out.

Last term for response: September 21, 2002, at the latest